

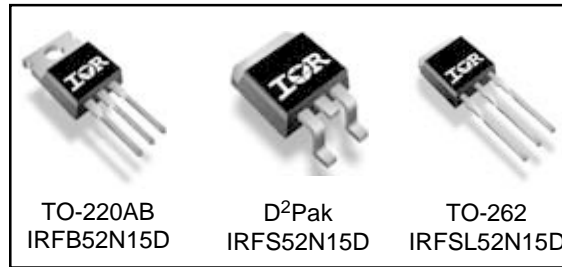
Applications

- High frequency DC-DC converters

| | | |
|------------------------|-------------------------------|----------------------|
| V_{DSS} | R_{DS(on) max} | I_D |
| 150V | 0.032Ω | 60A |

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|------------------------|-------|
| I _D @ T _C = 25°C | Continuous Drain Current, V _{GS} @ 10V | 60 | A |
| I _D @ T _C = 100°C | Continuous Drain Current, V _{GS} @ 10V | 43 | |
| I _{DM} | Pulsed Drain Current ① | 240 | |
| P _D @ T _A = 25°C | Power Dissipation ② | 3.8 | W |
| P _D @ T _C = 25°C | Power Dissipation | 320 | |
| | Linear Derating Factor | 2.1 | W/°C |
| V _{GS} | Gate-to-Source Voltage | ± 30 | V |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.5 | V/ns |
| T _J | Operating Junction and | -55 to + 175 | °C |
| T _{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw④ | 10 lbf•in (1.1N•m) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|------------------|---------------------------------------|------|------|-------|
| R _{θJC} | Junction-to-Case | — | 0.47 | °C/W |
| R _{θCS} | Case-to-Sink, Flat, Greased Surface ⑤ | 0.50 | — | |
| R _{θJA} | Junction-to-Ambient⑥ | — | 62 | |
| R _{θJA} | Junction-to-Ambient⑦ | — | 40 | |

Notes ① through ⑦ are on page 11

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|-------|----------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 150 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.16 | — | V/°C | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.032 | Ω | $V_{GS} = 10V, I_D = 36A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 3.0 | — | 5.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 150V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 30V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -30V$ |

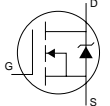
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|---------------------------------|------|------|------|-------|---|
| g_{fs} | Forward Transconductance | 19 | — | — | S | $V_{DS} = 50V, I_D = 36A$ |
| Q_g | Total Gate Charge | — | 79 | 120 | nC | $I_D = 36A$ |
| Q_{gs} | Gate-to-Source Charge | — | 25 | 37 | | $V_{DS} = 120V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | 34 | 51 | | $V_{GS} = 10V, \text{④}$ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 16 | — | ns | $V_{DD} = 75V$ |
| t_r | Rise Time | — | 47 | — | | $I_D = 36A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 28 | — | | $R_G = 2.5\Omega$ |
| t_f | Fall Time | — | 25 | — | | $V_{GS} = 10V, \text{④}$ |
| C_{iss} | Input Capacitance | — | 2770 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 590 | — | | $V_{DS} = 25V$ |
| C_{riss} | Reverse Transfer Capacitance | — | 110 | — | | $f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 3940 | — | | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 260 | — | | $V_{GS} = 0V, V_{DS} = 120V, f = 1.0\text{MHz}$ |
| $C_{oss\ eff.}$ | Effective Output Capacitance | — | 550 | — | | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V \text{ ⑤}$ |

Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|----------|---------------------------------|------|------|-------|
| E_{AS} | Single Pulse Avalanche Energy②⑥ | — | 470 | mJ |
| I_{AR} | Avalanche Current① | — | 36 | A |
| E_{AR} | Repetitive Avalanche Energy① | — | 32 | mJ |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|--|---|------|------|-------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 60 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) ①⑥ | — | — | 240 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.5 | V | $T_J = 25^\circ\text{C}, I_S = 36A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 140 | 210 | nS | $T_J = 25^\circ\text{C}, I_F = 36A$ |
| Q_{rr} | Reverse Recovery Charge | — | 780 | 1170 | nC | $di/dt = 100A/\mu s$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |

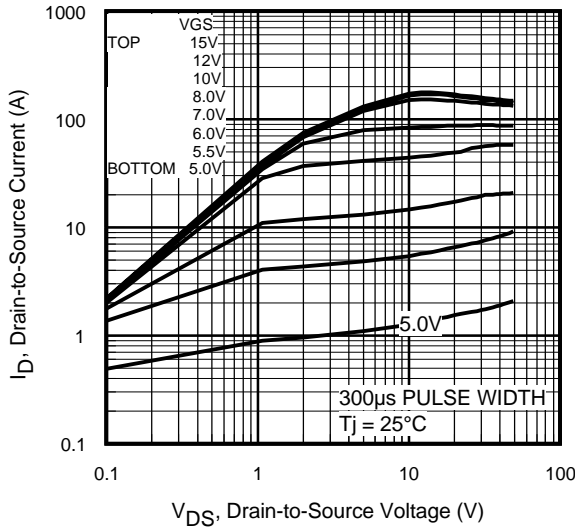


Fig 1. Typical Output Characteristics

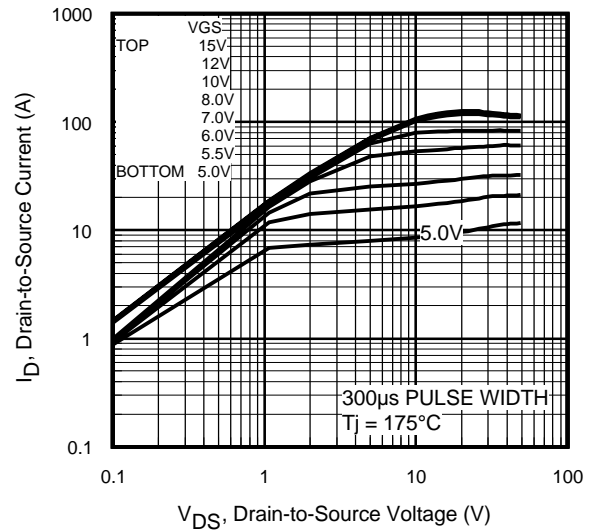


Fig 2. Typical Output Characteristics

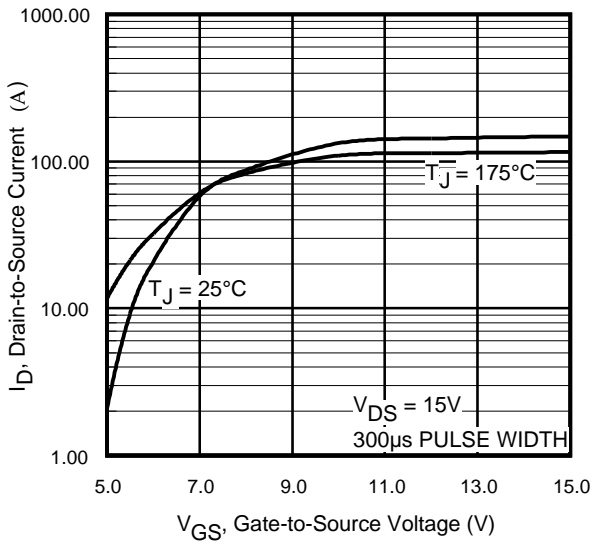


Fig 3. Typical Transfer Characteristics

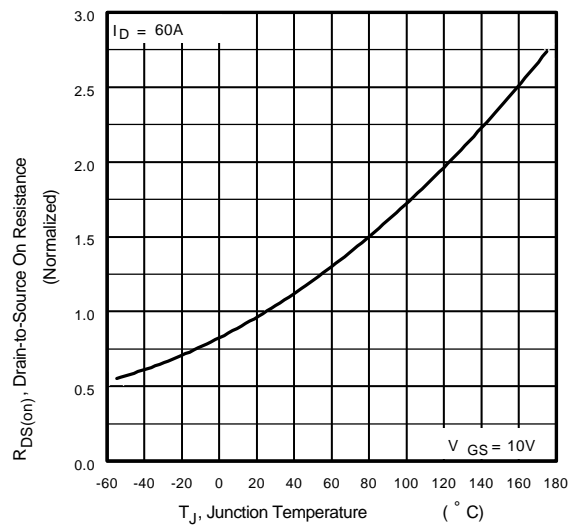


Fig 4. Normalized On-Resistance Vs. Temperature

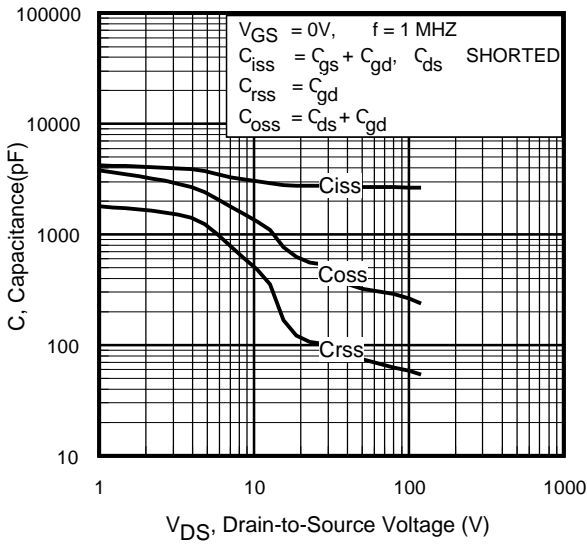


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

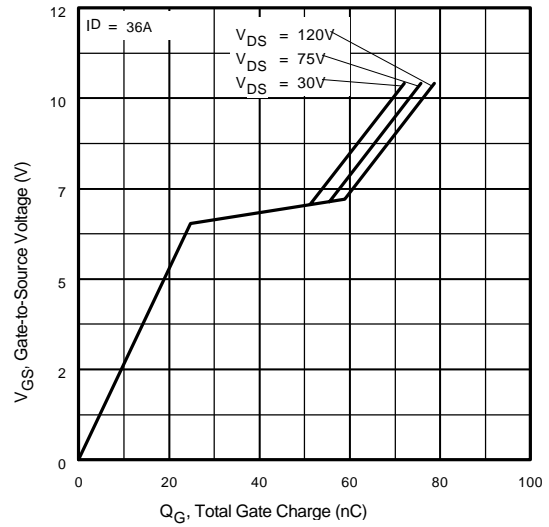


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

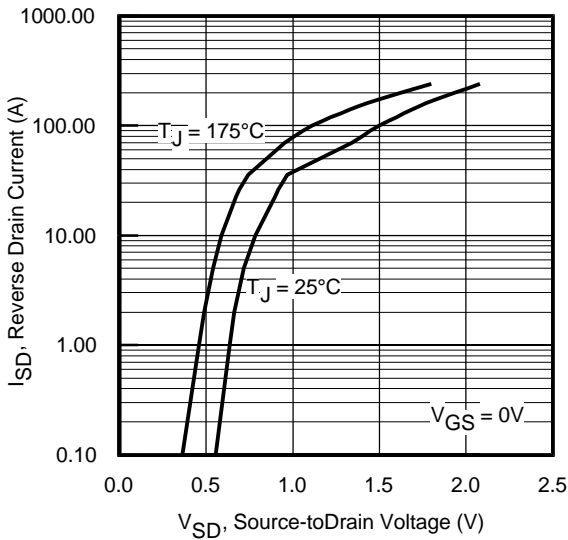


Fig 7. Typical Source-Drain Diode Forward Voltage

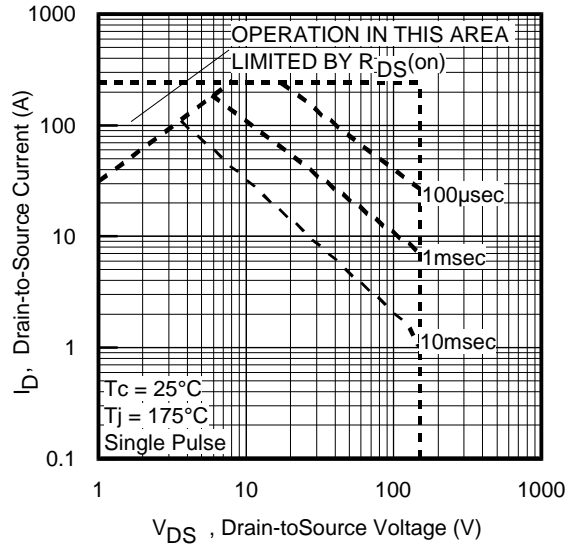


Fig 8. Maximum Safe Operating Area

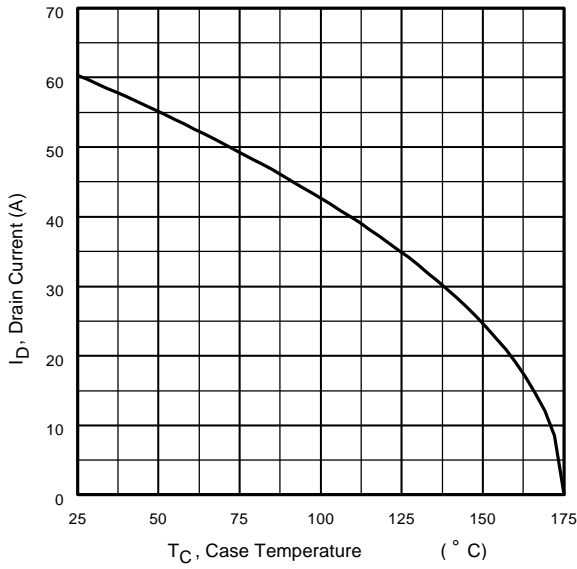


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit

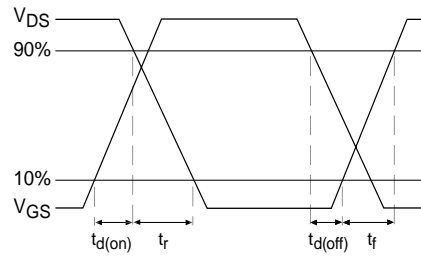


Fig 10b. Switching Time Waveforms

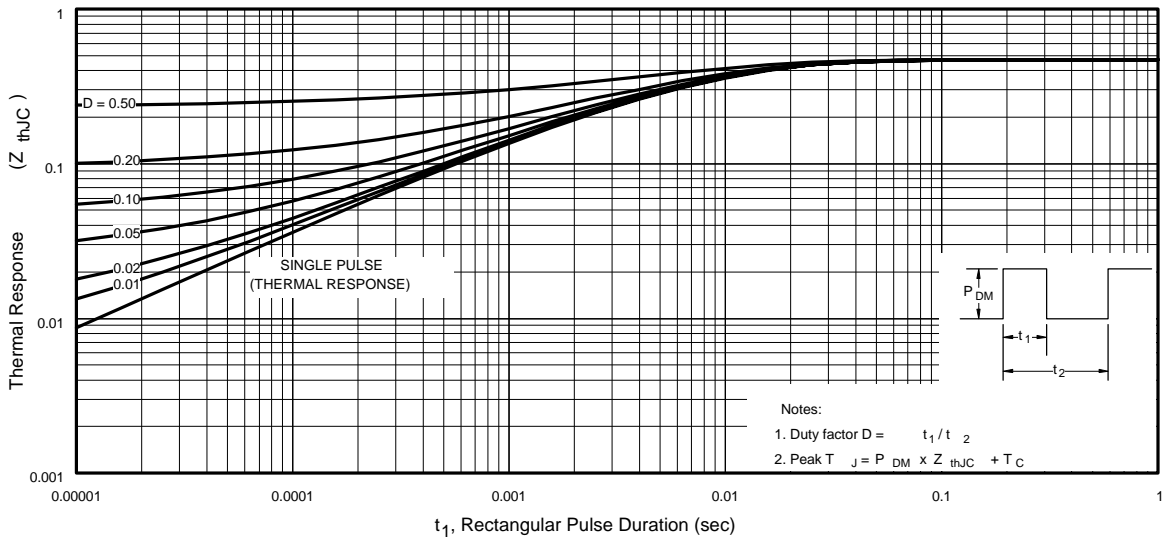


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFB/IRFS/IRFSL52N15D

International
IR Rectifier

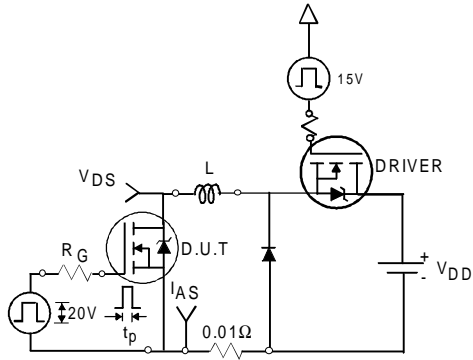


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms

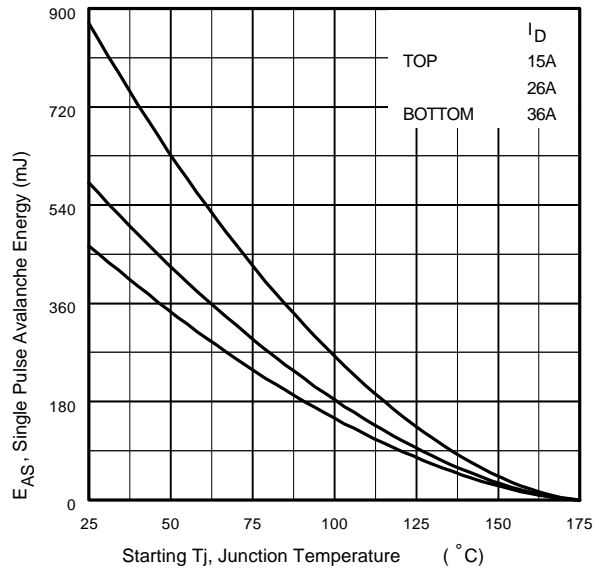


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

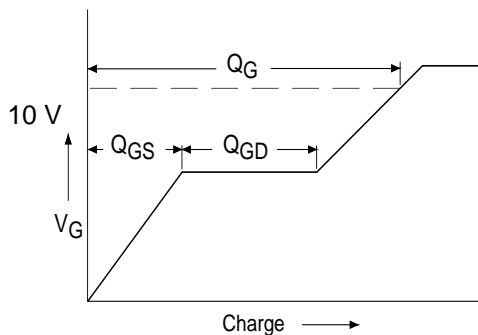


Fig 13a. Basic Gate Charge Waveform

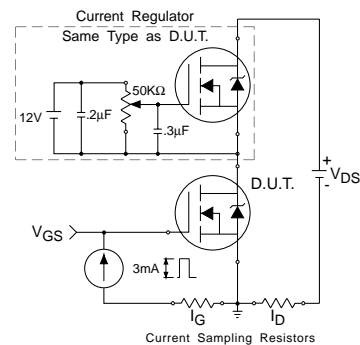


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

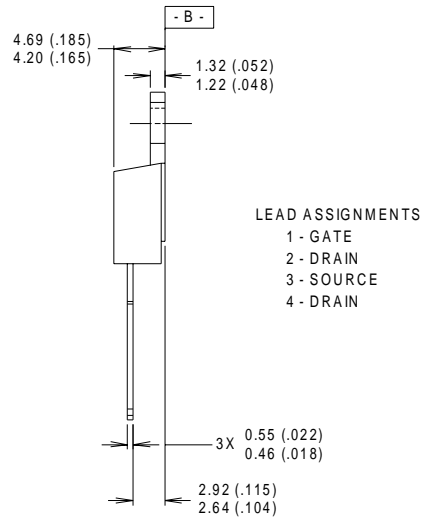
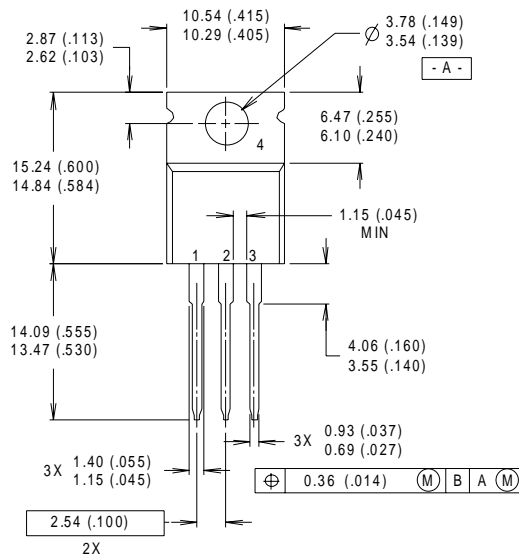
Fig 14. For N-Channel HEXFET® Power MOSFETs

IRFB/IRFS/IRFSL52N15D



TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



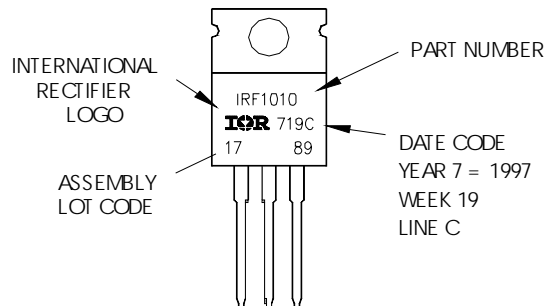
LEAD ASSIGNMENTS
 1 - GATE
 2 - DRAIN
 3 - SOURCE
 4 - DRAIN

NOTES:

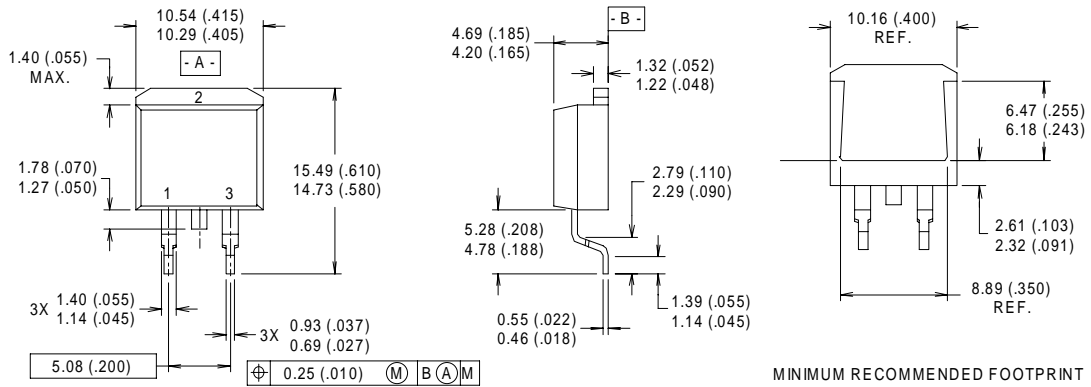
- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Package Outline



NOTES:

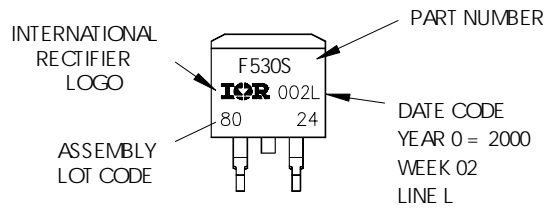
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

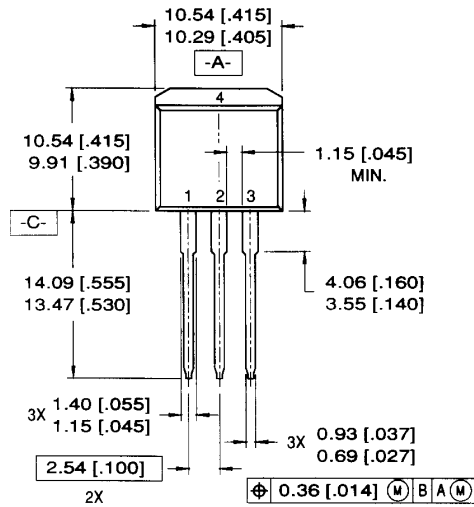
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
 LOT CODE 8024
 ASSEMBLED ON WW02, 2000
 IN THE ASSEMBLY LINE "L"



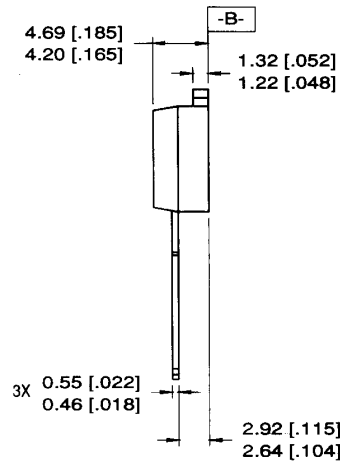
IRFB/IRFS/IRFSL52N15D

TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

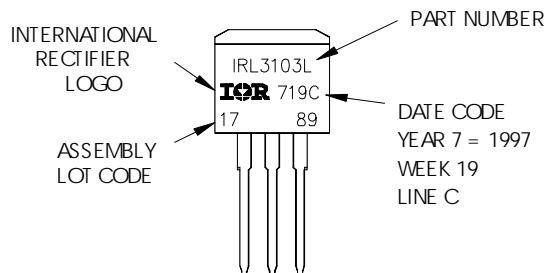


NOTES:

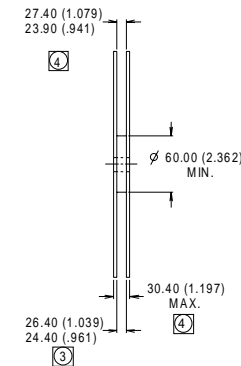
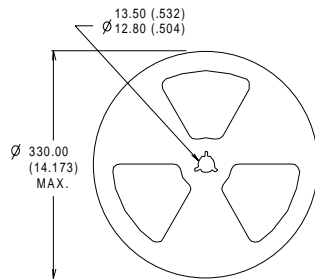
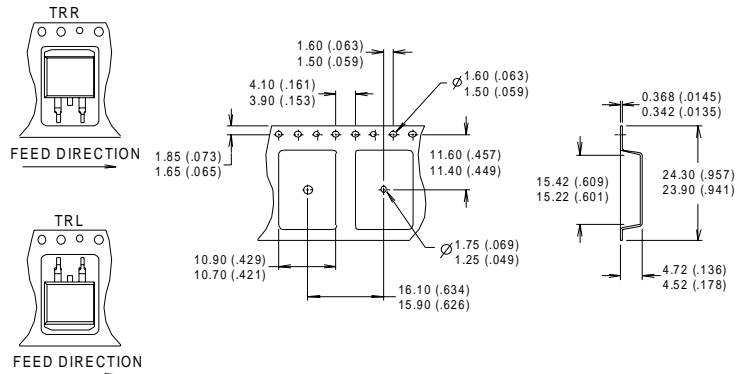
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON VW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



- NOTES:
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.72\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 36\text{A}$.
- ③ $I_{SD} \leq 36\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] (IRFB52N15D),
 & Industrial (IRFS/SL52N15D) market.
 Qualification Standards can be found on IR's Web site.